<table>
<thead>
<tr>
<th>Required Course:</th>
<th>ECE 36500 Introduction to the Design of Digital Computers</th>
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<tbody>
<tr>
<td>Credit and contact hours:</td>
<td>(3 cr.) Class 3, Lab 0</td>
</tr>
<tr>
<td>Prerequisite or corequisite:</td>
<td>P: ECE 362</td>
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<tr>
<td>Prerequisites by topic:</td>
<td>Digital devices, Number representation and codes, Computer programming.</td>
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<tr>
<td>Coordinator:</td>
<td>Stanley Chien, Professor of Electrical and Computer Engineering</td>
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<tr>
<td>Goals:</td>
<td>To teach junior or senior engineering students computer design and analysis techniques beginning with computer organization and ending with performance analysis.</td>
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<td>Outcomes:</td>
<td>Upon successful completion of the course, students should be able to</td>
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<td></td>
<td>1. Describe different types of instruction set architecture. [a]</td>
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<td></td>
<td>2. Design a control circuitry of a microprocessor. [a,c,e]</td>
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<td></td>
<td>3. Describe the concept of processor pipelining and its performance impact. [a,e]</td>
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<td>4. Describe the memory organization with caches and their performance impact. [a,e]</td>
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<td>5. Describe the key components of computer systems and their operation. [a,e]</td>
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<td>6. Design an Arithmetic Logic Unit. [a,c,e]</td>
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<td>Topics:</td>
<td>1. Basic computer organization (1 class)</td>
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<td>2. Instruction set design aspect (5 classes)</td>
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<td>3. I/O organization and devices (2 class)</td>
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<td>4. Processing unit organization (3 classes)</td>
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<td>5. Pipelined processor organization (3 classes)</td>
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<td>6. Memory/cache organization (6 classes)</td>
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<td>7. Arithmetic and logic unit design (3 classes)</td>
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<td>8. Exams (3 classes and final exam period)</td>
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<td>Computer usage:</td>
<td>Computer programming</td>
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<td>Laboratory projects:</td>
<td>None.</td>
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<tr>
<td>ABET category:</td>
<td>Engineering science 50% and engineering design 50%</td>
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<tr>
<td>Prepared by:</td>
<td>John Lee</td>
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<tr>
<td>Date:</td>
<td>September 26, 2014</td>
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</tbody>
</table>