A Synchronous Single Switch Inverter

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***Abstract*—Reducing the switch count and increasing the levels of voltage will increase the power inverters' quality and efficiency. Vector controls of inverters have been used to increase limited levels of output voltage; however, they create an increasingly complicated switching map that results in harmonics. This paper introduces the structure of a synchronized minimum switch-count inverter that is capable of generating infinite voltage levels. Four modes of operation were detected in creation of negative and positive polarity voltages. Transition modes provide polarity inversion capability. Compared to H-Bridge inverters, the efficiency of this power inverter can be increased by 7%. Simulation results demonstrate the successful operation of the inverter.**

***Index Terms*—Minimized switch count inverter, infinite voltage level, synchronized inverter.**

I. Introduction

Perfect inverters are required to efficiently generate pure sinusoidal waveforms [1] and operate in a wide range of loading conditions. To achieve this goal, several reduced switch count multi-level inverters [2-4] combined with soft-switching [5-10] and resonant circuits [6,8-13] have been introduced. As the number of voltage-levels increases, the generated waveform becomes closer to a perfect sinusoidal, increasing the system's power factor and efficiency. Several discrete hard-switching processes and complicated switching maps are required to create these voltage levels. Reducing the number of switches will require novel circuit topologies.

Much research has been conducted to achieve a reduced-switch count circuit. Often, these circuits replace transistors with diodes [14] or with a fault tolerant equivalent switch [15]. In case of a mixed load, these circuits have been developed to share a leg of the transistors i.e. five legs for 2 three-phase motors [16-18]. A significant reduction in switch count was achieved [14] by using three transistors and three-diodes. Soft-switching and resonant converters have also been introduced to decrease switching losses [19-22]. These circuits need accurately tuned resonators to operate at high frequency.

To achieve a robust DC power regulation, buck-boost Zeta converters have been used. They have shown high potential in microgrids and smart grids [23],[24]. These converters are also used in many industrial applications such as: LED lamp drivers [25], electronic ballast (EB) for fluorescent lamps [24], power rating correction and power quality improvements (PFC) [22], DC/DC converter interfaces between photovoltaic systems and the grid [26], power electronic interface between storage devices (battery and ultra-capacitor) in hybrid electric vehicles [27], AC inverters [28], and DC converter used for permanent magnet synchronous machines (PMSM) to interface for applications such as air conditioning systems, refrigerators, washing machines and medical equipment [29,30].

Several versions of these converters have been utilized to create advanced circuits such as fly-back converters while reducing the switch counts [31-35]. Zeta converters have also been used to create single, two, or three voltage-level inverters [36, 37]. They have also been used to directly convert DC to AC but with limited voltage-levels and increased switch counts [37]. In this design several Zeta converters have formed a 3 level output voltage [37]. Some guidelines have been developed to design these power converters [38]. However, to date, there is no power inverter capable of directly generating continuous-level voltages to result in pure sinusoidal and arbitrary waveforms.

To create a continuous-level voltage, advanced voltage tracking and voltage regulation in boost and buck modes of operation are required. Voltage polarity inversion and voltage boost operation are two of the limits in creation of desired AC voltages. The output voltage polarity of DC-DC converters does not change and boost circuits often result in a non-minimum phase behavior.

This paper, for the first time, reduces the count of high-frequency switching-transistors to one. The voltage-level will be continuously controlled to generate a pure sinusoidal and arbitrary waveform. In theory, infinite voltage-levels will be created for a perfect waveform without any need for switching map. A natural synchronized switching sequence will be created to generate the desired output voltage polarity and to reduce power losses. The capability of independently controlling the voltage amplitude and frequency provides enormous flexibility in generating arbitrary waveforms and operating with irregular input sources. The efficiency of proposed power inverter can also be increased by $4\eta/(1+3\eta)$, where η is the efficiency of a conventional H-bridge inverter considering similar conduction losses.

The organization of the paper is as follows: the circuit structure and modes of operation are illustrated in section II, and mathematical models are presented in section III. Simulation results are provided in section IV.

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II. Polarity Inversion Principle

Power electronic converters have numerous applications and have important role in overall system efficiency and performance. Accurate control of power converters are required to guarantee the voltage and frequency stability of the power system. Dynamic modeling of converters is required to understand the system operation and to design controller for power electronic converters. Many linear or nonlinear modeling techniques are used for mathematical expression of power converters. Nonlinear techniques such as component connection modeling and signal flow graph (SFG) [39], [40] are used for complicated circuits. State space averaging technique represents a linear technique in power electronic circuit modeling [3], [4], [41,42] with relatively accurate results. This paper uses state space averaging to identify the system models and better understand the modes of operations. Figure 1 shows the inverter structure of the synchronous single switch inverter.

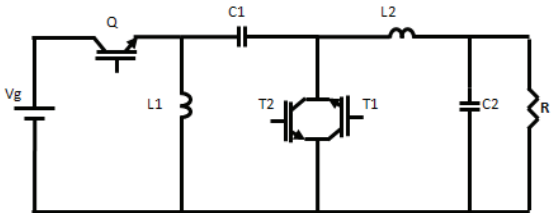


Fig. 1. Synchronous single switch inverter schematic diagram.

Modes of operation are generated when the status of switches change. When the switch Q is on, the input voltage is applied across L_1 and causes a linear increase of current to charge the inductor. In positive peak voltage, the input voltage and the charged capacitor C_1 will increase the load current through the inductor L_2. When the switch Q is off, L_1 charges C_1 through the synchronizing switch T_1, and L_2 supplies a forward current to the load generating positive voltage in the output. The inductor L_2 and capacitor C_2 create a filter, which lowers the output ripple. In negative peak voltage, the same procedure occurs, but to reverse the load current direction, synchronizing switch T_2 is turned on. This will introduce a transition mode to the system operation. The converter can continue operation in this mode by switching Q on and off accordingly. In CCM mode, the input and output voltages of the converter are related as follows:

$$\frac{V_{out}}{V_{in}} \quad \frac{D}{1-D}, \tag{1}$$

where $0 < D < 1$ is the converter's ideal duty cycle. The positive and negative signs are used for the positive peak and negative peak voltages respectively. In each half cycle, for values of D less than 0.5, the converter ideally operates in buck mode, and for values of D larger than 0.5 the converter ideally operates in boost mode. To maintain the CCM, the critical equivalent inductance of this circuit [43] is

$$L_{eq} < R(1-D)^2\left(\frac{T_S}{2}\right), \tag{2}$$

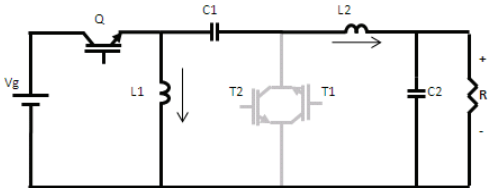
where,

$$L_{eq} = \frac{L_1 L_2}{L_1 + L_2}. \tag{3}$$

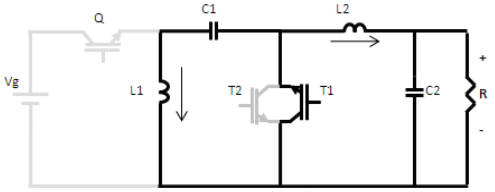
III. Modes of Operation and State Space Averaging Models

State space averaging is a dynamic modeling technique used for mathematical representation of converters. In this technique, the state space representation of each mode of operation is obtained, and the overall system is represented as an averaged system over a cycle. Since this inverter has a positive and a negative mode of operation, the model will be provided in these conditions.

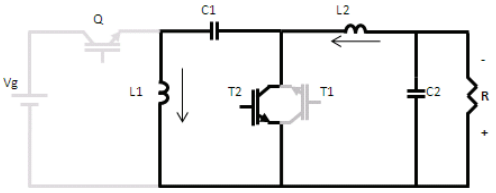
Figure 2 demonstrates the inverters' modes of operation. In positive voltage, the converter operates in modes I and II, and in negative peak it operates in modes III and IV. Therefore, two sets of equations can be written for this circuit, which can include internal resistances of the capacitors and inductors $r_{c1}, r_{c2}, r_{L1}, r_{L2}$.



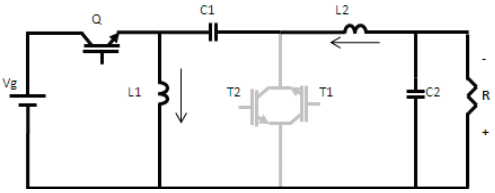
A) Mode I: Positive peak, Q and T1 are synchronized, Q: On, T1: Off.



B) Mode II: Positive peak, Q and T1 are synchronized, Q: Off, T1: On.



C) Mode III: Negative peak, Q and T2 are synchronized, Q: Off, T2: On.



D) Mode IV: Negative peak, Q and T2 are synchronized, Q: On, T2: Off.

Fig. 2. Modes of operation and transition from positive to negative peak voltage.

In Figure 2, circuit A shows the positive peak of inductor charging, B shows the inductor discharging and positive output voltage creation. Figure C shows the transition from positive peak to negative peak by switching the synchronizing transistor T_2 on. The current direction will change and the negative peak will be generated by Circuit D. This mode of operation charges the inductors with reverse current and provides a path to build up negative voltage of desired amplitude.

A. Positive Peak Voltage Generation

In Mode I, the switch Q is on and T_1 is off for duty cycle D

and in Mode II the switch is off and T_1 is on for period of $(1-D)$. Each set of state space system consist of five equations, four of which represent the four state variable dynamics $i_{L1}, i_{L2}, V_{c1}, V_{c2}$, and one equation to represent the output voltage of the circuit V_o. Equations representing mode I (Fig. 2.A) are as follows:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{V_g}{L_1} - \frac{r_{L1}}{L_1} i_{L1} \\ \frac{dv_{C1}}{dt} = -\frac{i_{L2}}{C_1} \\ \frac{di_{L2}}{dt} = \frac{V_g}{L_2} - i_{L2}\left(\frac{r_{L2}+r_{C1}+\frac{Rr_{C2}}{R+r_{C2}}}{L_2}\right) + \frac{V_{C1}}{L_2} - \frac{\frac{R}{R+r_{C2}}}{L_2} V_{C2}. \\ \frac{dv_{C2}}{dt} = \frac{\frac{R}{R+r_{C2}}}{C_2} i_{L2} - \frac{\frac{1}{R+r_{C2}}}{C_2} V_{C2} \\ V_0 = \frac{Rr_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} V_{C2} \end{cases} \quad (4)$$

In Mode II: Equations representing mode 2 (Fig. 2.B) are as follows:

$$\begin{cases} \frac{di_{L1}}{dt} = -i_{L1}\left(\frac{r_{L1}+r_{C1}}{L_1}\right) - \frac{V_{C1}}{L_1} \\ \frac{dv_{C1}}{dt} = \frac{i_{L1}}{C_1} \\ \frac{di_{L2}}{dt} = -i_{L2}\frac{(r_{l2}+\frac{Rr_{C2}}{R+r_{C2}})}{L_2} - \frac{\frac{R}{R+r_{C2}}}{L_2} V_{C2}. \\ \frac{dv_{C2}}{dt} = \frac{\frac{R}{R+r_{C2}}}{C_2} i_{L2} - \frac{\frac{1}{R+r_{C2}}}{C_2} V_{C2} \\ V_0 = \frac{Rr_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} V_{C2} \end{cases} \quad (5)$$

Considering $x=[i_{L1}, i_{L2}, v_{C1}, v_{C2}]$, the averaged state space model of positive peak voltage can be obtained as

$$\begin{cases} \dot{x} = A_{ave}^{+} x + B_{ave}^{+} u \\ V_o = C_{ave}^{+} x \end{cases} . \quad (6)$$

The positive peak averaged model parameters can be obtained as

$$A_{avg}^{+} = \begin{bmatrix} \frac{1}{L_1}(-r_{L1} - (1-D)\, r_{c1}) & 0 & \frac{D-1}{L_1} & 0 \\ & \frac{-(R+rc2)(Drc1+rl2)-Rrc2}{L_2(R+r_{C2})} & & \frac{-R}{L_2(R+r_{C2})} \\ 0 & -\frac{D}{C_1} & \frac{D}{L_2} & 0 \\ \frac{1-D}{C_1} & & 0 & -\frac{1}{C_2(R+r_{C2})} \\ 0 & \frac{R}{C_2(R+r_{C2})} & 0 & \end{bmatrix}$$

$$B_{avg}^{+} = \begin{bmatrix} \frac{D}{L_1} & \frac{D}{L_2} & 0 & 0 \end{bmatrix}^T \;,\; C_{avg}^{+} = \begin{bmatrix} 0 & \frac{Rr_{C2}}{(R+r_{C2})} & 0 & \frac{R}{R+r_{C2}} \end{bmatrix}. \quad (7)$$

B. *Negative Peak Voltage Generation*

In Mode III the switch is off and T_2 is on for duty cycle D, and in Mode IV the switch is on and T_2 is off for period $(1-D)$. Each set of state space system consist of five equations, four of which represent the four state variable dynamics $i_{L1}, i_{L2}, V_{c1}, V_{c2}$, and one equation to represent the output voltage of the circuit V_o. Equations representing mode III (Fig. 2.C) are as follows:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{V_g}{L_1} - \frac{r_{L1}}{L_1} i_{L1} \\ \frac{dv_{C1}}{dt} = \frac{-i_{L2}}{C_1} \\ \frac{di_{L2}}{dt} = -\frac{V_g}{L_2} - i_{L2}\left(\frac{r_{L2}+r_{C1}+\frac{Rr_{C2}}{R+r_{C2}}}{L_2}\right) + \frac{V_{C1}}{L_2} - \frac{\frac{R}{R+r_{C2}}}{L_2} V_{C2}\,. \\ \frac{dv_{C2}}{dt} = \frac{\frac{R}{R+r_{C2}}}{C_2} i_{L2} - \frac{\frac{1}{R+r_{C2}}}{C_2} V_{C2} \\ V_0 = \frac{Rr_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} V_{C2} \end{cases} \quad (8)$$

Mode IV (Fig. 2.D) has the following set of equations:

$$\begin{cases} \frac{di_{L1}}{dt} = -i_{L1}\frac{(r_{L1}+r_{C1})}{L_1} + \frac{V_{C1}}{L_1} \\ \frac{dv_{C1}}{dt} = -\frac{i_{L1}}{C_1} \\ \frac{di_{L2}}{dt} = -\frac{\frac{Rr_{C2}}{R+r_{C2}}}{L_2} i_{L1} - i_{L2}\frac{(r_{l2}+\frac{Rr_{C2}}{R+r_{C2}})}{L_2} - \frac{\frac{R}{R+r_{C2}}}{L_2} V_{C2}. \\ \frac{dv_{C2}}{dt} = \frac{\frac{R}{R+r_{C2}}}{C_2} i_{L1} + \frac{\frac{R}{R+r_{C2}}}{C_2} i_{L2} - \frac{\frac{1}{R+r_{C2}}}{C_2} V_{C2} \\ V_0 = \frac{Rr_{C2}}{R+r_{C2}} i_{L1} + \frac{Rr_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} V_{C2} \end{cases} \quad (9)$$

The averaged state space model of negative peak voltage can be obtained as

$$\begin{cases} \dot{x} = A_{ave}^{-} x + B_{ave}^{-} u \\ V_o = C_{ave}^{-} x \end{cases} . \quad (10)$$

The negative peak averaged model parameters can be obtained as

$$A_{avg}^{-} = \begin{bmatrix} \frac{1}{L_1}(-r_{L1} - (1-D) r_{C1}) & 0 & \frac{1-D}{L_1} & 0 \\ & -\frac{(r_{L2}+Dr_{C1})(R+r_{C2})+Rr_{C2}}{L_2(R+r_{C2})} & & \frac{-R}{L_2(R+r_{C2})} \\ -\frac{(1-D)Rr_{C2}}{L_2 2(R+r_{C2})} & \frac{-D}{C_1} & \frac{D}{L_2} & 0 \\ -\frac{1-D}{C_1} & & 0 & -\frac{1}{C_2(R+r_{C2})} \\ \frac{(1-D)R}{C_2(R+r_{C2})} & \frac{R}{C_2(R+r_{C2})} & 0 & \end{bmatrix}$$

$$B_{avg}^{-} = \begin{bmatrix} \frac{D}{L_1} & \frac{-D}{L_2} & 0 & 0 \end{bmatrix}^T \quad , C_{avg}^{-} = \begin{bmatrix} \frac{(1-D)Rrc_2}{C_2(R+rc2)} & \frac{Rrc_2}{C_2(R+rc2)} & 0 & \frac{R}{R+rc2} \end{bmatrix}. \quad (11)$$

Figure 3 demonstrates the voltages and currents of the components in the circuit when the polarity is changed. The circuit parameters are listed as follows $C_1 = 0.1\mu F, L_1 = 0.1\mu H, C_2 = 50\mu F, L_2 = 0.5\mu H$.

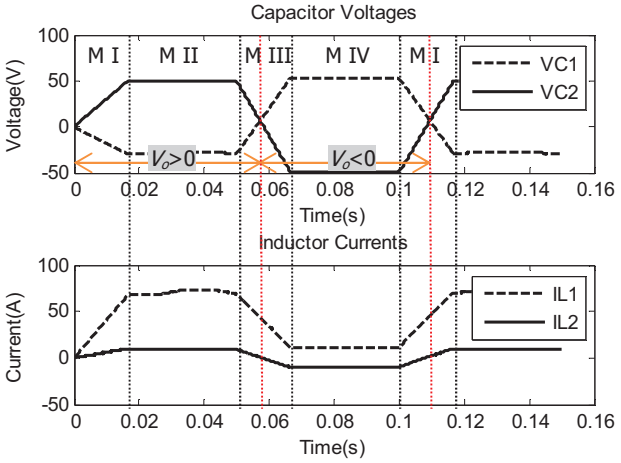


Fig. 3. Time interval of modes of operation.

In Figure 3, mode I shows the voltage of capacitor C_2 and currents of inductors L_1 and L_2 are increasing with positive

amplitudes. In mode II, the voltage and currents reach to a stable operation. In mode III the transition from positive peak to negative peak occurs. In mode IV, the current of inductor L_2 and voltage of capacitor C_2 become negative, and voltage of capacitor $C1$ becomes positive. Inductor of L_1 will have positive current in all modes of operation. A switching between modes I and II generates stable operation of positive peak voltage and modes of III and IV generate a negative peak voltage.

IV. Power Loss and Efficiency Analysis

Using the averaging technique, the switching power loss P_{SW} in one transistor resulting from the stored charge Q_r in the recovery time t_r in a cycle T_s can be calculated by

$$P_{SW} = \langle v_{in}(t)\rangle_{T_s}\left(\frac{Q_r}{T_s} + \frac{t_r}{T_s}\langle i_o(t)\rangle_{T_s}\right). \quad (12)$$

The efficiency of the power inverter can be calculated by [44]

$$\eta = \frac{P_{out}}{P_{in}} = \frac{1}{1+\frac{Q_r}{DT_sI}+\frac{t_r}{DT_s}}. \quad (13)$$

This efficiency improvement compared to H-bridge inverter, considering the same conduction loss and operating frequency, can be calculated by

$$\eta_{new} = \frac{4\eta}{1+3\eta}. \quad (14)$$

Therefore, as the number of high-frequency switching devices is decreased, the efficiency is increased. For instance, a 90%-efficient converter becomes 97.2% efficient.

V. Simulation Results and Discussion

The power inverter requires advanced active tracking controllers that are illustrated in Part II of this paper series. The results of computer simulations using SimPowerSystem toolbox of Matlab considering a large amount of circuit details are provided in this section of the paper.

A. Single-phase

A pure 110V, 60Hz sinusoidal waveform generated from the circuit is shown in Figure 4. As the figure illustrates, the output voltage tracks the reference signal in both positive and negative peaks. The output voltage is sensitive to load variations. At heavy loads the positive peaks generated some oscillations.

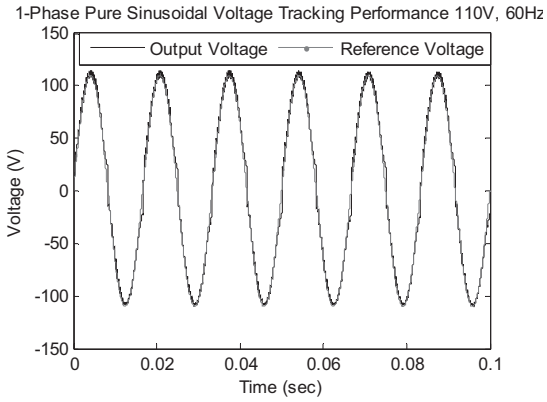


Fig. 4. Single-phase 110 V, 60Hz voltage generation. The output voltage and closely tracks the reference. The polarity inversion and amplitude generation are accomplished very accurately.

B. Bipolar Adjustable DC Output

The proposed power inverter can track any arbitrary reference. This reference can also be used to drive a DC motor at variable speed and different directions. Specifically, in applications where variable motor speed and constant directional changes are required, the proposed inverter can be very helpful. Figure 5 illustrates the voltage amplitude control and polarity inversion profile generated from the inverter. The inverter output voltage tracks the reference very accurately. This figure demonstrates that the inverter can operate as a buck-boost DC-DC chopper with the capability of inverting the voltage polarity on-demand. It also shows that asymmetrical voltages can be generated from the inverter. The output voltage perfectly tracks the reference and does not show overshoots or steady state errors.

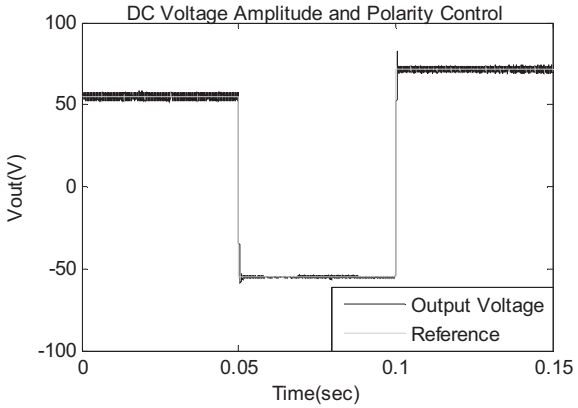


Fig. 5. Bipolar on-demand DC voltage generation. The power inverter was capable of independently controlling the amplitude and polarity of the voltage.

Conclusion

A new power inverter circuit was introduced that required only one high frequency switching transistor. The inverter used a synchronizing structure to change the voltage polarity on-demand. Therefore, real-time generation of infinite voltage levels was realized. The state space equations demonstrated a forth order system. The circuit also had four modes of operation to create alternating waveforms. The polarity inversion occurred when the set of synchronizing devices switched to reverse the current direction. The simulations results demonstrated the operation of the circuit and creation of desired voltage amplitude and polarity.

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